CENIDE & WIN Seminar Series on 2D-MATURE

DFG IRTG 2803 & NSERC CREATE

William S. Wong

University of Waterloo

"Process integration of MoS2 thin-film transistors for large-area electronics"

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William S. Wong is Professor in the Department of Electrical and Computer Engineering and Director of the Giga-to-Nanoelectronics Center at the University of Waterloo. His research is focused on electronic and optoelectronic materials and devices for large-area systems. Professor Wong received his Ph.D. in Materials Science and Mineral Engineering from the University of California, Berkeley in 1999. From 2000-2010 Wong was a Senior Member of Research Staff at the Palo Alto Research Center (formerly Xerox PARC) where he established their printed flexible electronics program. He is an author and co-author of more than 130 publications, with 75 invited talks and 85 issued patents. He is a member of the IEEE, the Materials Research Society, and was on the Editorial Board of IEEE Electron Device Letters from 2011-2020. Wong is also an invited organizer, elected committee member, and was Treasurer (2021-2023) of the Electronic Materials Conference. In 2023, Wong was elected to the Board of Directors for the Materials Research Society.

The increasing interest in the two-dimensional (2-D) layered transition metal dichalcogenide (TMDC) semiconductors has led to their potential use for high-performance large-area electronic applications. Challenges remain to integrate TMDC layers over large areas. Transfer methods have intrinsic limitations in areal coverage while direct deposition processes are still emerging. Two approaches will be presented to address these challenges. In the first methodology, few-layer structures (~ 3 monolayers) were fabricated using a layer transfer and dry etching process to thin multilayer (~ 60-90 nm thick) molybdenum disulfide (MoS_2) structures. The effect of plasma etching the TMDC surface and bulk defects in the layers on the device electrical performance and stability will be described. An observed degradation of the carrier transport and electrical stability were found to be due to the proximity of the etched surface to the device active region of the device. The results reveal the trade-offs of fabricating few-layer devices using exfoliation and dry etching approaches.

In a second investigation, hybrid organic/inorganic semiconductor inks were explored. The ink was prepared by mixing two different materials, MoS_2 nanosheets and solution-based poly(3-hexylthiopene-2,5-diyl) (P3HT). To enhance the level of exfoliation and stability of MoS_2 nanosheets in P3HT, the surfactant trichloro(dodecyl)silane (DDTS), was used to functionalize the MoS_2 surface. Inkjet printed thin-film transistors (TFTs) using the nanosheet suspension were found to enhance the field-effect mobility by approximately 3× compared to TFTs without the suspension. The introduced single-crystalline MoS_2 nanosheets in the P3HT matrix improved the electrical and structural properties of the inkjet-printed thin-film polymer. The enhancement of the electrical properties of the TFTs was determined to be due to a structural change in the

thin-film semiconductor. The observed current-voltage changes were correlated to measurable structural alterations in the semiconductor thin film characterized by X-ray diffraction, atomic force microscopy, and UV-visible absorption spectroscopy.